A Wideband Low-Noise Downconversion Mixerwith Positive-Negative Feedbacks

Hadi Naderian*
RF Circuit, M.Sc, Electrical Engineering Department, Shahid Bahonar University of Kerman
h.naderian@eng.uk.ac.ir
Ahmad Hakimi
RF Circuit and Microwave Components, Ph.D, Electrical Engineering Department, Shahid Bahonar University of Kerman
Hakimi@uk.ac.ir

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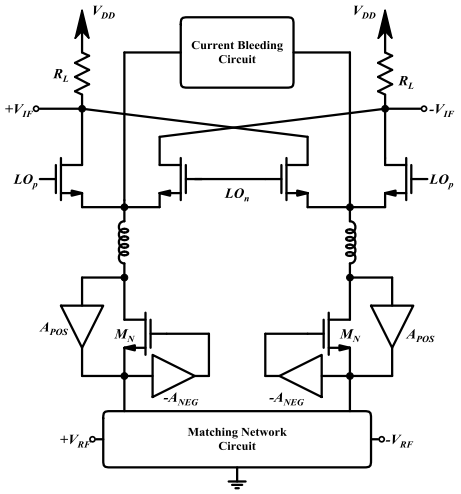
Abstract
This paper presents a wideband low-noise mixer in CMOS 0.13-um technology that operates between 2–10.5 GHz. The mixer has a Gilbert cell configuration that employs broadband low-noise trans conductors designed using the negative-positive feedback technique used in low-noise amplifier designs. This method allows broadband input matching. The current-bleeding technique is also used so that a high conversion gain can be achieved. Simulation results show excellent noise and gain performance across the frequency span with an average double-sideband noise figure of 2.9 dB and a conversion gain of 15.5 dB. It has a third-order intermodulation intercept point of -8.7 dBm at 5 GHz.

Keywords: Current-Bleeding, Feedback, Low-Noise, Noise Cancellation, Wideband.

1. Introduction

Active mixers based on the Gilbert cell configuration often exhibit a large amount of noise. This leads to strict requirements for the noise figure (NF) of the low-noise amplifier (LNA) preceding the mixer such that a particular signal-to-noise ratio can be achieved. This usually requires at least one very low-noise LNA that has enough gain and noise performance to mitigate the noise added by the mixer. Power consumption is also a problem as the LNA NF decreases when larger transistors are used. However, these requirements can be much relaxed or the LNA can be removed if the mixer NF is low enough. The Gilbert cell mixer has been widely used in integrated circuit (IC) design even though it exhibits moderate noise. However, its NF can be drastically reduced by combining the LNA and mixer into a single component. Narrowband low-noise mixers have been proposed in other works [1]–[4], where the transconductors were replaced by inductive-degenerated LNAs.



Block diagram of proposed mixer circuit.

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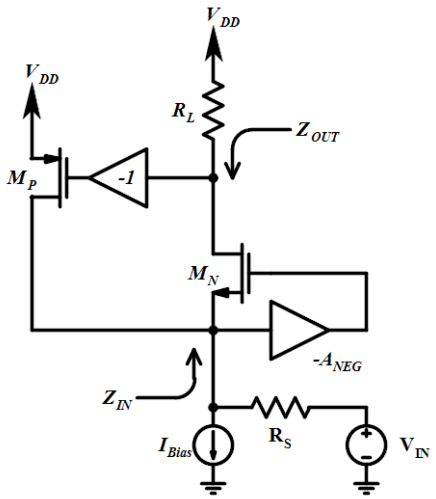


Simplified block diagram of transconductor.

To convert a Gilbert cell into a wideband low-noise mixer, the trans conductors must be wideband in terms of NF, gain, and input matching. Many broadband and UWB LNAs have been proposed [5]–[7]. In [5], an active feedback approach was used to achieve broadband input matching and gain. The circuits in [6] and [7] use filters to achieve broadband input matching and low noise performance. Another broadband LNA design method is the noise-cancelling technique [8], which has been used for mixer in [9].

A common-gate (CG) LNA has been widely investigated because it features superior bandwidth, linearity, stability, and robustness to PVT variations compared to a common-source (CS) topology [10]. In spite of these advantages, the dependence of gain and NF on the restricted transconductance (gm) makes this topology unsuitable for various wireless applications. The input impedance of a CG LNA is simplified as 1/gm, and the noise factor is inversely proportional to gm [11]. In order to achieve high gain and low NF, gm should be increased, which deteriorates the 50Ω input impedance matching for a conventional CG LNA.

In this paper to achieve high gain and low NF without sacrificing bandwidth, linearity, and power consumption, a differential gm-boosted CG transconductors with a positive-negative feedback technique is proposed. The proposed mixer with output buffers delivers a maximum conversion gain of 15.5 dB, a minimum NF of 2.6 dB, an IIP3 of -8.7 dBm, and 22.44mW power consumption.

2. Circuit Description

The proposed wideband low-noise mixer block diagram is shown in Figure 1. The mixer based on the Gilbert cell topology with some modifications. The mixer is comprised of four building blocks: positive-negative feedback transconductors, peaking inductors, current bleeding and switching pairs. A detailed design analysis of the positive-negative feedback transconductors block is provided first, followed by a description of each block.

2.1 Positive- Negative Feedback Trans conductors

The proposed topology, shown in Figure 2, consists of cross-coupled capacitors in negative and PMOS transistors in positive feedback branches in a differential CG configuration.RL is the mixer load resistor, assuming there is no loss through the switch, and the tail capacitance of the off switch is negligible compared to the load resistor. The differential signals flow to the sources of the NMOS transistors, and are also cross-coupled to the gates of the opposite NMOS transistors through capacitors, which results in a shunt-series negative feedback path [12]-[15]. The outputs of the NMOS transistors are coupled to the sources of the opposite NMOS transistors creating a shunt-shunt positive feedback loop.

The input impedance is obtained as

$$Z_{\mathrm{IN}} = \frac{1}{g_{mMn}(1+A_{NEG})(1-A_{POS})}. \quad (1)$$

using input shunt-negative and shunt-positive feedback theory [16]. ANEG, which is approximately given by $C_C/(C_C+C_{gs})$, is almost unity. Positive feedback is equivalent to $g_{mMp}R_L$, can be varied from 0 to 1 for an arbitrary choice of g_{mMp} required to achieve an input matching condition. The output impedance is given by

$$Z_{OUT} = \frac{R_L\left[r_{ds}+R_S\left\{1+(1+A_{NEG})g_m r_{ds}\right\}\right]}{R_L+r_{ds}+R_S\left\{1+(1+A_{NEG})g_m r_{ds}\right\}(1-A_{POS})} \quad (2)$$

r_{ds} is the output impedance of transconductance transistor. While A_{POS} is increased, the output impedance, as well as g_{mMn} for the input matching, can be increased. In this architecture, the voltage gain is given by

$$A_V = \frac{g_m(1+A_{NEG})}{2}\times\frac{2}{\pi} \times\frac{R_L\left[r_{ds}+R_S\left\{1+(1+A_{NEG})g_m r_{ds}\right\}\right]}{R_L+r_{ds}+R_S\left\{1+(1+A_{NEG})g_m r_{ds}\right\}(1-A_{POS})} \quad (3)$$

where $2/\pi$ is an approximation of switching gain. With the help of gm boosting through the

capacitor cross-coupling (CCC) negative feedback, effective transconductance (G_M) is the same as the NMOS transconductance itself. As a result, the voltage gain ($=G_M.Z_{OUT}$) can be high with relatively low power consumption through the large Z_{OUT} and large G_M.

The NF of the circuit can be computed considering thermal channel noise of transconductance transistors and load noise. For high IF thermal noise is dominant, so flicker noise of switching stage was neglected [17]. In this case [18],

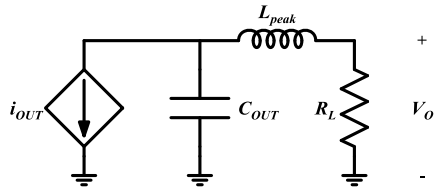
$$F = 1 + \frac{\gamma(1-A_{POS})}{\alpha(1+A_{NEG})} + g_{mMp}R_S\frac{\gamma}{\alpha} + \frac{R_S}{R_L}(2-A_{POS})^2 \quad (4)$$

Where γ is the MOS transistor thermal noise coefficient, α is defined as the ratio of g_{mMn} to the zero-bias drain conductance g_{d0}. The second term represents the channel noise contribution of g_{mMn}, which can be greatly reduced through A_{NEG} as well as A_{POS}. The channel noise of M_N flows to the gate and source of an opposite M_N with the same phase through C_C and the positive path, respectively. Thus, the combination of positive feedback and the negative feedback loop contributes to channel-noise cancellation. The third and fourth terms show the noise induced by M_P in the positive feedback path, and the load, respectively. The noise due to M_P can be decreased by using small g_{mMp}, and the load noise is reduced by A_{POS}.

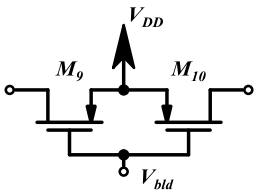
2.2 Inductive Peaking

The mixer bandwidth can be significantly affected by the large output capacitance from transconductors, as well as from the bleeding circuit and switching pairs. Inductive peaking can be used for bandwidth extension. Series peaking is used in this design and the peaking inductors are placed between the switching pairs and the transconductors, as shown in Figure 1.

To understand the operation of these inductors, a simplified circuit is shown in Figure 3 when only one of the switches is on. Preceding the mixer core is the transconductors, which can be approximated by a voltage-controlled current source; C_{out} is the collective output capacitance from the transconductor and the bleeding circuit; R_L is the mixer load resistor, assuming there is no loss through the switch, and the tail capacitance of the off switch is negligible compared to the load resistor.The basic theory of inductive peaking can be explained with Figure 3 and the step response. Imagine the circuit without the inductor, the rise time at the output is about 2.2RC, if the rise time is defined to be the elapsed time between 10%–90% of the final output voltage value. To decrease the charge time, i.e., increase the bandwidth, the inductor is used. At t=0, there is a sudden step change in the current source.



Two-pole series peaking network [9].



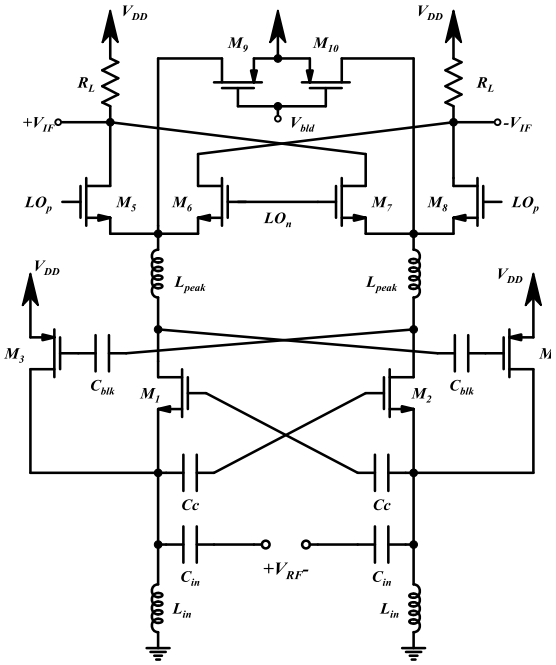
PMOS bleeding circuit.

The high impedance of the inductor decouples the resistor from the capacitor, which means all the current goes into charging the capacitor. Therefore, the rise time decreases, and hence the bandwidth is enhanced.

2.3 Switching Pairs and Current Bleeding

In general, increasing the bias current of the RF transconductance stage makes higher gain and better linearity possible, but a larger LO switching current causes voltage headroom issue. Therefore, as shown in Figure 4, the static current bleeding technique is implemented by using two PMOSFETs to reduce the bias current of the LO switches [19].

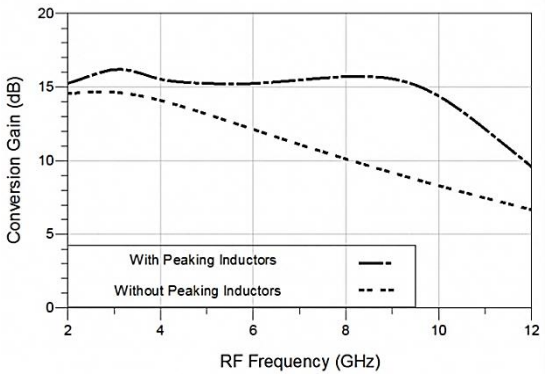
The gain of the mixer is maximized by fast switching similar to a square wave. The turn-on voltage for the switching pairs is proportional to their overdrive voltage, and it needs to be low to ensure fast switching. By having a lower overdrive voltage, the size of the load resistors can be increased to achieve an even higher gain.



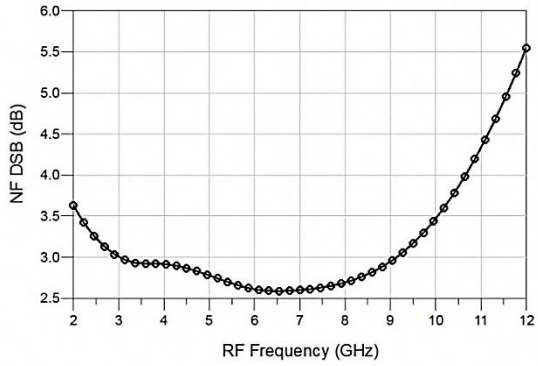
Complete circuit schematic of the proposed mixer.

3. Simulation Results

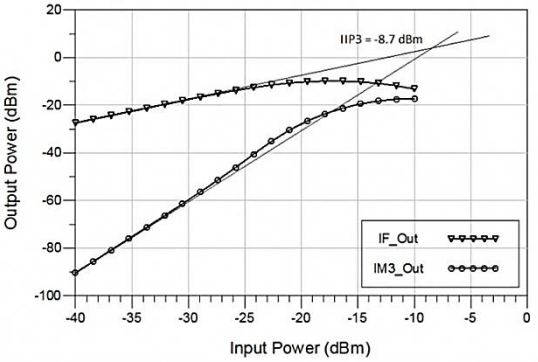
The mixer was designed using TSMC's CMOS 0.13-µm technology. Simulation was run using Advanced Design System (ADS) software. The mixer is designed to operate between 2–10.5 GHz with a local oscillator (LO) power of 0 dBm. Quality factor of peaking inductors and input inductors has been set to 4 and 10, respectively.



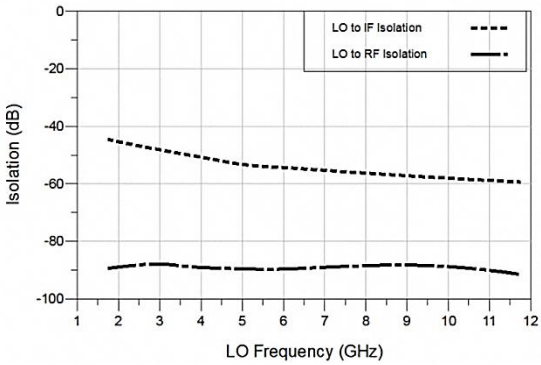
Conversion gain of the proposed mixer.



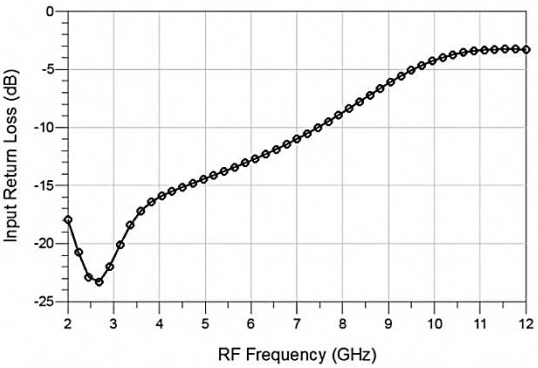
DSB Noise Figure simulation result.



Output powers of the IF and the IM3 product with the input at 5 GHz.



Port-to-Port isolations versus LO frequency.



Input matching of the mixer.

For all simulation results, the IF is always kept at a constant 250 MHz, while the RF and LO frequencies are being changed together with the LO being 250 MHz lower than the RF. Two source-follower buffers were used to combine

the differential IF signal into a single-ended output.

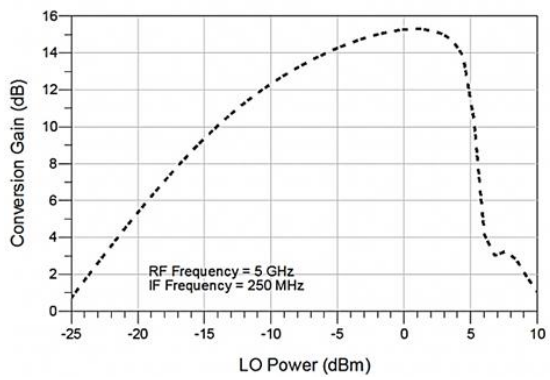
The conversion gain of the mixer is measured across the input frequency ranging from 2 to 10.5 GHz. The input RF power was kept at -40 dBm. Figure 6 shows the conversion gain simulated results. This plot also includes the simulated result without the peaking inductors. The importance of the peaking inductors can be clearly seen in this plot, where there is a much sharper gain roll off compared to the simulated result with peaking.

When characterizing the noise performance of a mixer, either the double- or single-sideband NF can be used [15]. Figure 7 shows the simulated double-sideband NF of the mixer versus input frequency. The circuit has a low and relatively flat NF across bandwidth. The minimum value of NF is 2.6 dB at 6.5 GHz and the maximum is 3.9 dB at 10.5 GHz.

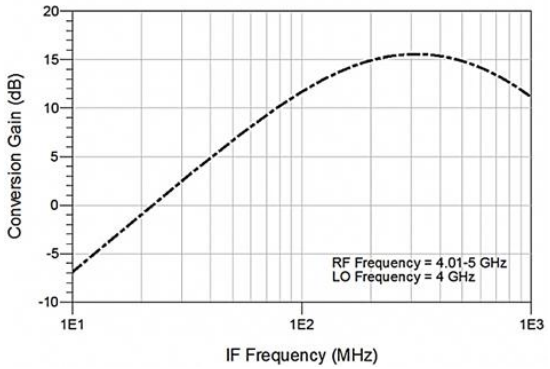
The third-order intermodulation intercept point (IIP3) of the mixers was simulated. To simulate the IIP3, a two-tone signal separated by 1 MHz was used. Shown in Figure 8 is the simulated IF and third-order.

Table I Comparison of Wideband Down-Converters with This Work

Parameters	This Work	[20]	[9]	[21]	[22]	[23]z
CMOS Technology	0.13 um	0.13 um	0.13 um	65 nm	90 nm	0.18 um
RF Bandwidth (GHz)	2 - 10.5	3.1 - 10.6	1 - 5.5	2 - 8	0.1 – 3.85	0.2 - 13
Conversion Gain (dB)	15.5	9.8 - 14	17.5	23 (Voltage)	12.1	9.9
NF DSB (dB)	2.9	14.5 - 19.6	3.9	4.5	8.4-11.5 (SSB)	11.7
IIP3 (dBm)	-8.7	-11	+0.84	-7	N/A	-10
LO Power (dBm)	0	3	0	N/A	1	5
Voltage Supply (V)	1.2	1.2	1.5	1.2	1.2	0.8
Power Consumption (mW)	22.44	1.85	34.5	39	9.8	0.88



Conversion gain versus LO power.

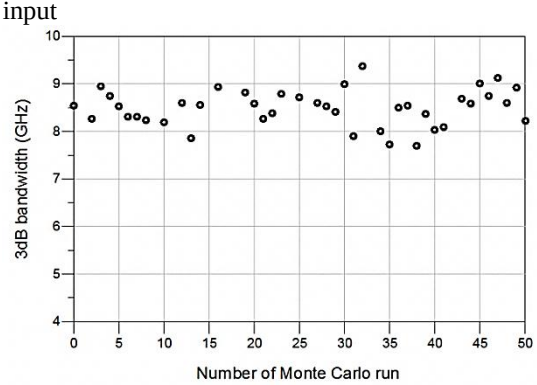


Simulation results of IF bandwidth.

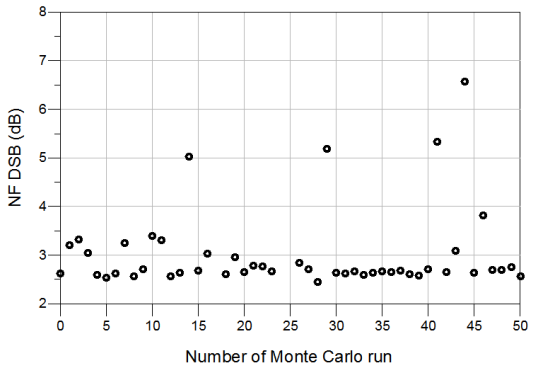
intermodulation (IM3) output powers with the input RF frequency at 5 GHz. The extrapolated IIP3 was -8.7 dBm.

The LO-to-RF port-to-port isolation and LO-to-IF port-to-port isolation were simulated. Since the LO is 250 MHz lower than the RF, the isolation was simulated from 1.75 GHz to 11.75 GHz. Figure 9 shows the simulated mixer ports isolation.

Figure 10 shows the input return loss. The simulation results of conversion gain versus LO input



Result of Monte Carlo analysis of the mixer bandwidth.



Result of Monte Carlo analysis of the mixer bandwidth

power is shown in Figure 11 which shown that 0 dBm LO power is optimum value for this circuit. The simulation of IF bandwidth is shown in Figure 12 that shows 3-dB bandwidth of conversion gain at the IF port is about 700 MHz. The mixer core draws a total current of 3.54 mA and buffers draws 15.6 mA from a 1.2-V supply, respectively.

The impact of the process and mismatch variations on the mixer frequency response and noise figure has been evaluated by utilizing the well-known Monte-Carlo statistical analysis. Device variations are fluctuations in MOS parameters and include, Effective gate length (L_{eff}), Threshold voltage (V_t), Thickness of the gate oxide (T_{ox}), and the drain/source region parasitic resistance (R_{dsw}) [24]. The Monte-Carlo simulation of the mixer bandwidth and noise figure is depicted in Figure 13 and Figure 14, respectively. In the noise figure Monte-Carlo analysis has been performed in 6 GHz RF frequency.

Table 1 shows a comparison between this work and recently published broadband down-converters in CMOS. The mixer outperforms others in terms of noise performance while still having a comparable gain. Their circuit structures are also different. This work and [9] have a current reuse structure, whereas [21] is a LNA Mixer TIA in cascade and [22] is a folded mixer with a folded low-noise transconductors. [23] uses bulk-injection and switched biasing techniques together.

4. Conclusion

A double-balanced Gilbert-type mixer based on the positive-negative feedback technique was designed using a 0.13-um CMOS process covering the frequency band between 2 and 10.5 GHz. The noise-cancelling technique allows broadband input matching and noise cancellation at the same time. Together with the current-bleeding technique, a high conversion gain was also achieved. Moreover, parasitic capacitances cancellation was done by adding an extra inductor between switching and transconductance stages to obtain better NF and gain performance. The circuit exhibits 2.9 dB average noise figure while the mixer core draws only 3.54 mA form a 1.2-V supply.

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